IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	M. Kapur et al.
Docket No.:	YOR920030306US1
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Group:	2138
Examiner:	Saqib Javaid Siddiqui
Title:	Self-Synchronizing Pseudorandom Bit Sequence Checker

APPEAL BRIEF

Commissioner for Patents
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Sir:

This Appeal Brief is submitted in response to the non-final Office Action dated March 21, 2007, in which the Examiner reopened prosecution responsive to the Appeal Brief filed by Applicants (hereinafter "Appellants") on December 4, 2006. Appellants hereby appeal the rejection of claims 1-17 of the above-referenced application. A new Notice of Appeal was filed on June 21, 2007.

REAL PARTY IN INTEREST

The present application is assigned to International Business Machines Corporation, as evidenced by an assignment recorded August 28, 2003 in the U.S. Patent and Trademark Office at Reel 14479, Frame 375. The assignee, International Business Machines Corporation, is the real party in interest.

RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1-17 stand rejected under 35 U.S.C. §112, first paragraph. Claims 1-17 stand rejected under 35 U.S.C. §112, second paragraph. Claims 1-17 stand rejected under 35 U.S.C. §103(a). Claims 1-17 are appealed.

STATUS OF AMENDMENTS

There was a minor amendment filed subsequent to the final rejection, which addressed an alleged antecedent basis issue in dependent claim 9. In an Advisory Action dated October 27, 2006, the Examiner indicated that the amendment was entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The method comprises the steps of delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device, and prohibiting propagation of the detected error bit in the delayed PRBS, wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

As explained at page 2, lines 1-7, of the present specification, the methodology advantageously provides that, for a given clock cycle, the presence of an error bit in the PRBS generated by the device is detected. The error bit represents a mismatch between the PRBS input to the device and the PRBS output from the device. Then, propagation of the error bit is prohibited for subsequent clock cycles. The prohibition step/operation may serve to avoid multiple errors being counted for a single error occurrence and/or masking errors in the PRBS output by the device.

The present specification provides an illustrative embodiment of the elements of claim 1 at page 6, line 10, through page 8, line 7, in the context of FIGs. 4 and 5.

More particularly, FIG. 4 illustrates a PRBS checker according to an embodiment of the present invention. As shown, PRBS generator 410 is coupled to the input of DUT 420. PRBS

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More particularly, FIG. 4 illustrates a PRBS checker according to an embodiment of the present invention. As shown, PRBS generator 410 is coupled to the input of DUT 420. PRBS checker 430 is coupled to the output of DUT 420. PRBS generator 410 may be the same as PRBS generator 310 of FIG. 3. Also, DUT 420 may be a communication circuit or channel under test.

PRBS checker 430 includes a shift register chain including R0, R1 and R2. Checker 430 also includes XOR gate RX0, XOR gate RX1, XOR gate RX2, no input sequence detector 432, zero detector 434, one detector 436, error counter 438 and display count 440.

The use of the shift registers is an example of the claimed step of "delaying the PRBS received by the device to generate a delayed PRBS." Thus, the incoming bits from DUT 420 are shifted directly into the shift register chain which is of the same length as the generator shift register. The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0. The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1. This is an example of the claimed step of "detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device."

An error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2. This is an example of the claimed step of "prohibiting propagation of the detected error bit in the delayed PRBS." Zero detector 434 is employed to allow enough clock cycles for the generator data to flush (pass) through the DUT and initialize the full shift register length (R0 through R2). Zero detector 434 generates an enable signal after completing its operation to turn on one detector 436. Error counter 438 counts the errors and display count 440 displays the error count. The error counter may be a conventional binary synchronous counter.

Independent claim 6 recites an apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The apparatus comprises a memory, and at least one processor coupled to the memory and operative to: (i) delay the PRBS received by the device to generate a delayed PRBS; (ii) detect the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by

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the device; and (iii) prohibit propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

It is to be understood that the apparatus of claim 6 recites similar steps as method claim 1. Therefore, an illustrative summary of the claimed operations performed by the apparatus are described above with respect to claim 1. Further, page 9, line 8, through page 10, line 5, describe an illustrative processor/memory arrangement for implementing the claimed invention.

Independent claim 11 recites an article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The article comprises a machine readable medium containing one or more programs which when executed implement the steps of delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device, and prohibiting propagation of the detected error bit in the delayed PRBS, wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

It is to be understood that the article of claim 11 recites similar steps as method claim 1. Therefore, support for the steps performed by the article are described above. Further, page 9, line 8, through page 10, line 5, describe an illustrative machine readable medium arrangement for implementing the claimed invention.

Independent claim 12 recites an apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device. The apparatus comprises a shift register chain, a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS, and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

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As described in detail above, FIG. 4 depicts an illustrative embodiment of the claimed invention recited in independent claim 12. PRBS checker 430 is an example of the recited apparatus for checking the accuracy of an output PRBS generated by a device in response to an input PRBS received by the device. PRBS checker 430 includes a shift register chain including R0, R1 and R2 (an example of the recited shift register chain). XOR RX1 is an example of a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS. In response to detection of the presence of the error bit, the error in the DUT output stream is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2 (an example of the recited at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Whether claims 1-17 fail to comply with the enablement requirement under 35 U.S.C. §112, first paragraph.

(2) Whether claims 1-17 are indefinite under 35 U.S.C. §112, second paragraph.

(3) Whether claims 1, 2, 4-7, 9-12 and 17 are unpatentable under 35 U.S.C. §103(a) over alleged Applicants Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent No. 4,627,057 to Schmidt et al. (hereinafter "Schmidt").

(4) Whether claims 3 and 8 are unpatentable under 35 U.S.C. §103(a) over AAPA in view of Schmidt further in view of U.S. Patent No. 6,215,876 to Gilley (hereinafter "Gilley").

(5) Whether claims 13-16 are unpatentable under 35 U.S.C. §103(a) over AAPA in view of Schmidt further in view of U.S. Patent Application Publication No. 2002/0063553 to Jungerman (hereinafter "Jungerman").

ARGUMENT

Appellants incorporate by reference herein the disclosure of their previous responses filed in the present application, namely, the responses dated March 31, 2006 and September 29, 2006.

(1) Whether claims 1-17 fail to comply with the enablement requirement under 35 U.S.C. §112, first paragraph.

With regard to the §112, first paragraph rejection of claims 1, 6, 11 and 12, it is commonly known in the art that "[s]hift registers can be used as simple delay circuits." ("Shift register." Wikipedia, The Free Encyclopedia. 25 May 2007, 23:55 UTC. Wikimedia Foundation, Inc. 15 Jun 2007 <http://en.wikipedia.org/w/index.php?title=Shift_register&oldid=133531151>). The delaying step as recited in claim 1 is illustrated in FIG. 4 of the present specification. PRBS checker 430 (an example of a device receiving a PRBS) includes a shift register chain including R0, R1, and R2. The input PRBS received by the PRBS checker is delayed, the incoming bits from DUT 420 are shifted directly into the shift register chain, i.e., the input PRBS is delayed. (Specification, page 6, lines 17-24).

Regarding the prohibiting step of claims 1, 6, 11 and 12, support for the limitation is shown on page 6, line 24 through page 7, line 6 of the present specification. After the output of registers R2 and R1 are fed to XOR gate RX0, the output of RX0 is compared with the incoming bit from DUT 420. The comparison is done using XOR gate RX1. If an error in the DUT output stream is detected, propagation of the detected error bit is prohibited. The detected error bit is immediately flagged as a "1" at the output of RX1. This "1" is delayed by one clock cycle in one detector 436 and is used to invert the output of register R0 using XOR gate RX2. The Examiner states at page 4 of the final Office Action: "that is not prohibition that is error correction." Appellants respectfully assert that the present application illustrates error bit correction as one way of prohibiting propagation of the error bit. The use of the term prohibition is clearly defined in the application and thus supports the use of such term in the claims.

In claim 12, the apparatus for checking the accuracy of an output PRBS is the PRBS checker 430 and the device which generates an output PRBS is DUT 420. Therefore the input PRBS is the

input to DUT 420, the output PRBS is the output of DUT 420, and what the PRBS checker checks for is accuracy.

  Accordingly, the rejection of claims 1-17 under §112, first paragraph, should be withdrawn.

  (2) Whether claims 1-17 are indefinite under 35 U.S.C. §112, second paragraph.

  With regard to the §112, second paragraph rejection of claims 1, 6, 11 and 12, the delayed PRBS is not the same signal as the PRBS received by the PRBS checker. For the sake of clarification, Appellants point out that the "device" recited in claims 1, 6 and 11 refers to the PRBS checker 430, whereas the "device" recited in claim 12 refers to DUT 420.

  With regard to claims 1, 6 and 11, as noted above, the delayed PRBS is generated when the incoming bits from DUT 420 are shifted directly into the shift register chain. Thus, as different signals, an error can be detected by comparing a portion of the delayed PRBS with a portion of the PRBS received by the device. The relationship between the PRBS received by the device and the delayed PRBS is that the PRBS received by the checker is that which is being shifted directly into the shift register chain, thus generating the delayed PRBS. The PRBS is outputted from the DUT and shifted directly into the shift register chain, the outputs of registers R2 and R1 are fed to XOR gate RX0, and the output of RX0 is compared with the incoming bit from DUT 420. (See the specification at page 6, lines 10-26).

  In claim 12, the accuracy of PRBS received by a DUT is checked at the PRBS checker, not the DUT. It may further assist the Examiner's understanding to refer to page 5, lines 3-11, that explains how the PRBS generator (310 and 410) operates, and thus how the PRBS checker functions.

  Accordingly, the §112, second paragraph rejection of claims 1-17 should be withdrawn.

  (3) Whether claims 1, 2, 4-7, 9-12 and 17 are unpatentable under 35 U.S.C. §103(a) over alleged Applicants Admitted Prior Art (hereinafter "AAPA") in view of U.S. Patent No. 4,627,057 to Schmidt et al. (hereinafter "Schmidt").

  With regard to the §103(a) rejections, Appellants initially note that a proper case of obviousness requires that the cited references when combined must "teach or suggest all the claim

limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Appellants submit that the Examiner has failed to establish a proper case of obviousness in the §103(a) rejection of claims 1, 2, 4-7, 9-12 and 17 over AAPA and Schmidt, in that the AAPA and Schmidt references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention.

Independent claim 1 is directed to a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device. The method comprises the steps of delaying the PRBS received by the device to generate a delayed PRBS, detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device, and prohibiting propagation of the detected error bit in the delayed PRBS, where the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

Further, independent claim 12 recites apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising: a shift register chain; a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

In Appellants' previous response, it was pointed out that, according to the present specification at page 4, line 14, through page 6, line 9, there are two major types of PRBS checkers. The first type uses a very simple technique as shown in FIG. 2 of the present application. PRBS checker 230 includes a synchronization detector (synchronizing circuit) 232, a local PRBS generator

234 and a comparator circuit 236. Synchronization detector 232 looks for a known pattern in the incoming stream. Once detector 232 detects the known pattern, detector 232 turns on local PRBS generator 234. Local generator 234 and the generator (e.g., 110 in FIG. 1, but not expressly shown in FIG. 2) at the input of DUT 220 are designed to be identical. After synchronization is achieved, the two generators are expected to produce identical bit streams. The comparator circuit 236 detects any mismatches caused due to DUT 220. A major drawback of this technique is the penalty caused due to the synchronizing circuit. These circuits are difficult to build, consume a lot of power as they run at the full rate of incoming data, and their size grows with the length of the generation polynomial.

Appellants respectfully point out that this first approach is the approach taken by Schmidt, i.e., the locally generated signal is the "test signal" described in Schmidt at column 4, lines 29-48.

A second approach uses a self-synchronizing technique as shown in FIG. 3 of the present application. This approach eliminates the need for a synchronizing circuit and local PRBS generation. As explained, PRBS generator 310 includes shift registers T0, T1 and T2, which form a shift register chain. The output of T2 and T1 is fed to an XOR (exclusive OR) gate TX0. The output of TX0 is fed to the input of register T0. Thus, a PRBS of length seven is formed. At any given time, there are three bits in the generator registers (T0 through T2). These three bits identify a single state out of seven states that the generator cycles through. Any new state can be derived from a previous state by the XOR and shift operation. This fundamental principle of generation is used in the self-synchronizing checker. PRBS checker 330 includes a shift register chain including R0, R1 and R2. Checker 330 also includes XOR gate RX0, XOR gate RX1 and error counter 332. The incoming bits from DUT 320 are shifted directly into the shift register chain which is of the same length as the generator shift register. The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0. The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1. Under ideal circumstances, the incoming bit is the same as the RX0 output. Any errors introduced by DUT 320 are then counted by error counter 332.

Appellants point out that this second approach is the approach taken by the AAPA.

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As further explained in the present application, this second technique has three major drawbacks. First, multiple errors are flagged for a single occurrence. For example, if the DUT sends a bit stream with a single error bit, an error will be flagged at the output of XOR gate RX1 for the first time. This error bit will then propagate from the input of register R0 to the output of R1 after two clock events. When the erroneous bit arrives at the output of R1, the erroneous bit will flag an error for the second time. An error flag will be raised for the third time when this bit reaches the output of R2. Thus, a single error will be flagged three times. A second drawback is that the technique of FIG. 3 masks errors. For example, if in any given incoming stream there are two error bits separated by one, two or three bit positions, these will cancel each other, thus showing no error at all. This is referred to as masking. A third drawback of the technique of FIG. 3 is that if the DUT sends out only zero bits, no error is flagged.

A fundamental reason for flagging of multiple errors and masking is the propagation of an erroneous bit through the shift registers. The present invention realizes that to prevent such an occurrence, the error bit propagation has to be stopped. For example, in a binary system, this error bit can be inverted to its correct value.

The inventions recited in amended independent claims 1, 6 and 11, and original claim 12 address the stated problems with the existing self-synchronizing approach (FIG. 3) by "prohibiting propagation of the detected error bit in the delayed PRBS" (claims 1, 6 and 11), and by "at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain" (claim 12).

The Examiner states that "AAPA does not explicitly teach prohibiting propagation of the error bit for subsequent clock cycles," and refers to the Schmidt reference as teaching the prohibiting step. The Examiner looks to the Schmidt reference to supplement the above-noted deficiencies of AAPA as applied to claim 1. The claimed invention recites an explicit step of "prohibiting propagation of the detected error bit in the delayed PRBS." It is understood that the claim is explicitly stating that the propagation of the detected error bit in the delayed PRBS is being prohibited. Illustrative examples of how this is done are mentioned above and described in the

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present specification, e.g., in a binary system, the error bit is inverted to its correct value thus prohibiting propagation of the error bit. The fact that Schmidt switches to some kind of safe mode, is not the same as prohibiting propagation of the detected error bit in the delayed PRBS, as the claimed invention recites. Furthermore, Schmidt does not even teach delaying a PRBS.

The Schmidt reference fails to supplement the above-noted deficiencies of AAPA as applied to claim 1. Accordingly, it is believed that the combined teachings of AAPA and Schmidt fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining AAPA and Schmidt in the manner proposed. The Examiner provides the following statement of motivation beginning at page 7, third paragraph of the Office Action:

> It would have been obvious to one skilled in the art to prohibit the propagation of the error bit within the testing procedure of AAPA, since one skilled in the art would have recognized that prohibiting the propagation of the error bit will prevent the error bit from effecting the whole system and ensure that the testing apparatus continues proper operation without involving the error bit.

Applicants respectfully submit that this is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, 127 S.Ct. 1727, 1741, 82 U.S.P.Q.2d 1385, 1396 (U.S., Apr. 30, 2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine AAPA and Schmidt to produce the particular limitations in question.

Furthermore, there is no suggestion in AAPA that the self-synchronizing technique disclosed in AAPA would work when combined with the local-generator type (non-self-synchronizing) PRBS checker disclosed in Schmidt. Accordingly, the proposed combination appears to be based primarily on hindsight, with the Examiner attempting to reconstruct the claimed arrangement from disparate references.

For at least the above reasons, Appellants assert that claims 1, 2, 4-7, 9-12 and 17 are patentable over AAPA and Schmidt.

Appellants further assert that dependent claims 2, 4, 5, 7, 9, 10 and 17 recite patentable subject matter in their own right.

By way of example, claims 4, 9 and 17 recite detecting the non-presence of a PRBS from the device. The Office Action cites Schmidt at column 6, lines 4-10. However, such portion of Schmidt mentions nothing about an actual, express step of detecting the non-presence of a PRBS from the device. Schmidt refers to an "impermissible condition 00000000." However, this condition is not detected, nor is it necessarily representative of the non-presence of a PRBS.

(4) Whether claims 3 and 8 are unpatentable under 35 U.S.C. §103(a) over AAPA in view of Schmidt further in view of U.S. Patent No. 6,215,876 to Gilley (hereinafter "Gilley").

Appellants assert that claims 3 and 8 are patentable over the AAPA/Schmidt/Gilley combination for at least the reasons given above with respect to claims 1 and 6. Gilley fails to remedy the deficiencies of AAPA and Schmidt.

Appellants further assert that dependent claims 3 and 8 recite patentable subject matter in their own right.

Claims 3 and 8 recite that the prohibition step further comprises correcting the error bit. The Office Action at page 10 states that "Schmidt et al. does not explicitly teach the correction of the error bit." Then, the Office Action cites a error correction being disclosed in Gilley at column 7, lines 1-5. Column 7, lines 1-5 states that "[h]owever, if the number of errors is large (e.g. ≥4 bit errors) (66/76), it is concluded that the predicted IV is wrong (76), and appropriate action can be taken (78), which might consist of dropping crypto-sync and attempting to re-acquire it from the received IV (80)." The relied-upon portion of Schmidt does not teach or suggest the correction of the error bit. However, even if properly combinable, Appellants do not see how these two references teach or suggest the claim limitations that a prohibition step/operation comprises correcting the error bit. There is no prohibition step/operation disclosed by the combination.

Further, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

(5) Whether claims 13-16 are unpatentable under 35 U.S.C. §103(a) over AAPA in view of Schmidt further in view of U.S. Patent Application Publication No. 2002/0063553 to Jungerman (hereinafter "Jungerman").

Appellants assert that claims 13-16 are patentable over the Schmidt/Jungerman combination for at least the reasons given above with respect to claim 12. Jungerman fails to remedy the deficiencies of Schmidt.

Appellants further assert that dependent claims 13-16 recite patentable subject matter in their own right.
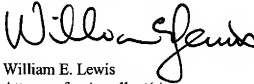
Claim 13 recites a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain. Claim 14 recites wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector. Claim 15 recites an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS. Claim 16 recites an error count display coupled to the error counter for displaying the error count.

While the Examiner admits that AAPA and Schmidt fail to disclose such claim limitations, the Office Action attempts to combine AAPA and Schmidt with a non-analogous reference that discloses a system for displaying a waveform on an error performance analyzer (Jungerman). Even if Jungerman were to show an error counter or error count display, it has nothing to do with checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device.

Thus, Appellants assert that the Examiner has failed to provide legally sufficient rationale for combining the two references.

In view of the above, Appellants believe that claims 1-17 are in condition for allowance, and respectfully request withdrawal of the various §112 and §103(a) rejections.

Respectfully submitted,

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APPENDIX

1. A method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the method comprising the steps of:

delaying the PRBS received by the device to generate a delayed PRBS;

detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and

prohibiting propagation of the detected error bit in the delayed PRBS;

wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

2. The method of claim 1, wherein the prohibition step serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device.

3. The method of claim 1, wherein the prohibition step further comprises correcting the error bit.

4. The method of claim 1, further comprising the step of detecting the non-presence of a PRBS from the device.

5. The method of claim 1, wherein the device is one of a communication circuit and a communication channel.

6. Apparatus for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the apparatus comprising:

a memory; and

at least one processor coupled to the memory and operative to: (I) delay the PRBS received by the device to generate a delayed PRBS; (ii) detect the presence of an error bit in the PRBS

received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and (iii) prohibit propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

7. The apparatus of claim 6, wherein the prohibition operation serves to avoid at least one of multiple errors being counted for a single error occurrence and masking errors in the PRBS received by the device.

8. The apparatus of claim 6, wherein the prohibition operation further comprises correcting the error bit.

9. The apparatus of claim 6, wherein the processor is further operative to detect the non-presence of a PRBS from the device.

10. The apparatus of claim 6, wherein the device is one of a communication circuit and a communication channel.

11. An article of manufacture for checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, comprising a machine readable medium containing one or more programs which when executed implement the steps of:

delaying the PRBS received by the device to generate a delayed PRBS;

detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and

prohibiting propagation of the detected error bit in the delayed PRBS;

wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device.

12. Apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising:

a shift register chain;

a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and

at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

13. The apparatus of claim 12, further comprising a second logic detector coupled to the at least one logic detector for allowing enough clock cycles for the input PRBS to pass through the device and initialize the full length of the shift register chain.

14. The apparatus of claim 13, wherein the second logic detector generates an enable signal after completing its operation so as to turn on the at least one logic detector.

15. The apparatus of claim 12, further comprising an error counter coupled to the logic gate for counting errors detected between the input PRBS and the output PRBS.

16. The apparatus of claim 15, further comprising an error count display coupled to the error counter for displaying the error count.

17. The apparatus of claim 12, further comprising a third logic detector coupled to the shift register chain for detecting the non-presence of a PRBS from the device.

EVIDENCE APPENDIX

None.

<u>RELATED PROCEEDINGS APPENDIX</u>

None.